Please enter the following claims:

1. (currently amended) A memory device configured to perform multi-bank operations comprising:

a plurality of memory banks including at least a first and second memory bank respectively controlled by a first and a second redundancy replacement means; and

a redundancy allocation means for allocating redundancy elements by way of performing a comparison of ~~comparing~~ data bits read out from said first memory bank against corresponding expected data, said data bit comparison occurring only when said first bank is addressed during a multi-bank operation.

2. (original) The memory device recited in claim 1, further comprising second means for comparing the data bits read out of said second memory bank against corresponding expected data, said comparison occurring only when said second bank is addressed during a multi-bank operation.

3. (currently amended) The memory device recited in claim 2, wherein a ~~the~~ period of said comparison is longer than the bank-to-bank access cycle time of said multi-bank operation.

4. (original) The memory device recited in claim 2, wherein said means selects either the first or the second bank to perform said comparison, and wherein said comparison is enabled only when the selected bank is addressed.

5. (original) The method device as recited in claim 1 wherein said expected data is provided when prompted by a read command, said read command being delayed by a predetermined read latency.

PAGE 4/12 * RCVD AT 11/7/2005 11:56:39 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2738300 * CSID:845 892 6363 * DURATION (mm-ss):03-22

6. (original) The memory device as recited in claim 1, wherein said comparison means is a dynamic exclusive OR circuit comprising:

a first transistor having a gate, source, and drain respectively coupled to said data, to a first node, and to a second node,

a second transistor having a gate, source, and drain respectively coupled to the complement of said expected data, to a first voltage source, and to said first node,

a third transistor having a gate, source, and drain respectively coupled to the complement of said data, to a third node, and to said second node, and

a fourth transistor having a gate, source, and drain respectively coupled to said expected data, to said first voltage source, and to said third node, such that said second node follows said first voltage source only if no match of said data to said expected data occurs.

7. (original) The memory device as recited in claim 6, wherein said expected data and the complement thereof remain at low until said comparison means is enabled, and either of said expected data and complement thereof switches to high when said comparison means are enabled.

8. (original) The memory device as recited in claim 6, wherein said expected data and the complement of said expected data are generated by a single expected data and an enabling signal.

9. (original) The memory device as recited in claim 6 further comprising a fifth transistor having a gate, source and drain respectively coupled to a line carrying a first signal to said second voltage source, and to said second node, wherein said second node is precharged to said second voltage prior to performing said data comparison by controlling said first signal.

PAGE 5/12 * RCVD AT 11/7/2005 11:56:39 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2738300 * CSID:845 892 6363 * DURATION (mm-ss):03-22

10. (original) The memory device as recited in claim 9, wherein the detection result of said second node is held until said first signal precharges said second node.

11. (original) The memory device as recited in claim 10, further comprising:

at least one second circuit to enable a data comparison for a different data bit, and

means for OR'ing all said data comparison circuits, wherein a fail is identified by one of said data comparison circuits.

12. (currently amended) The memory device as recited in claim 1, wherein a ~~the~~ time required for allocating a redundancy during a multi-bank operation exceeds the bank-to-bank clock cycle.

13. (currently amended) The memory device as recited in claim ~~claimed in~~ 1, wherein a ~~the~~ time required for allocating a redundancy to a predetermined domain during a multi-bank operation extends over one random access cycle.

14. (original) The memory device as recited in claim 1 further comprising means for fetching address bits only when comparing means compares data bits read out from said memory bank against corresponding expected data.

15. (currently amended) A memory device configured to perform multi-bank operations comprising:

a plurality of memory banks wherein at least two banks are supported by separate redundancy replacement means;

PAGE 6/12 * RCVD AT 11/7/2005 11:56:39 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2738300 * CSID:845 892 6363 * DURATION (mm-ss):03-22

identifying means for identifying one bank of said plurality of memory banks;

a data comparison means; and

redundancy allocation ~~enabling~~ means for enabling at least two of said banks in a multi-bank mode for accepting expected data, ~~and for generating an enable signal~~, wherein said redundancy allocation ~~enabling~~ means enables said data comparison means to detect if data bits read from one of said ~~bank matches its~~ banks match corresponding expected data only when said identification means identifies said corresponding bank during said multi-bank operation.

16. (currently amended) The memory device as recited in claim 15 further comprising an address storage means ~~(640)~~ for storing address bits therein only when said identification means identifies a predetermined bank during the multi-bank operation.

17. (original) The memory device as recited in claim 15 further comprising:

a plurality of address registers, each of which supports corresponding banks;

means for enabling a redundancy allocation to a predetermined memory bank during said multi-bank operation;

means for switching said redundancy allocation to another of said memory banks and for switching an address register to said another memory bank; and

means for enabling the redundancy allocation to all of said memory banks during the multi-bank operation by applying an addressing pattern to all of said memory banks during the multi-bank operation.

PAGE 7/12 * RCVD AT 11/7/2005 11:56:39 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2738300 * CSID:845 892 6363 * DURATION (mm-ss):03-22

18. (original) A method for allocating a redundancy in a memory device configured for a multi-bank operation, comprising the steps of:

sub-dividing said memory device into a plurality of memory banks, wherein at least two banks are supported by different redundancy replacement means;

enabling said at least two banks in a multi-bank mode;

identifying said redundancy domain during the multi-bank mode and accepting expected data; and

enabling a data comparison of data bits read from one of said banks and matching said data bits to corresponding expected data only when said bank is identified and addressed during said multi-bank operation.

19. (original) The method recited in claim 18, wherein enabling said data comparison is realized by a dynamic exclusive-OR circuit, said dynamic exclusive-OR circuit comprising:

a first transistor having a gate, source, and drain respectively coupled to data, to a first node, and to a second node;

a second transistor having a gate, source, and drain respectively coupled to the complement of said expected data, to a first voltage source, and to said first node;

a third transistor having a gate, source, and drain respectively coupled to the complement of said data, to a third node, and to said second node; and

a fourth transistor having a gate, source, and drain respectively coupled to said expected data, to said first voltage source, and to said third node, such that said second node follows said first voltage source only if no match of said data to said expected data occurs.

PAGE 8/12 * RCVD AT 11/7/2005 11:56:39 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2738300 * CSID:845 892 6363 * DURATION (mm-ss):03-22

20. (currently amended) The method recited in claim 19 ~~18~~ further comprising a fifth transistor having a gate, source and drain respectively coupled to a line carrying a first signal, to said second voltage source, and to said second node, wherein said second node is precharged to said second voltage prior to performing said data comparison by controlling said first signal.

21. (currently amended) The method recited in claim 19 ~~18~~, further comprising the step of maintaining the detection result of said second node from the initial time when said data comparison is enabled to a time when said first signal precharges said second node.

22. (currently amended) The method recited in claim 18, wherein a ~~the~~ time required for the allocation of a redundancy during a multi-bank operation exceeds a bank-to-bank clock cycle.

23. (currently amended) The method recited in claim 18, wherein a ~~the~~ time required for the allocation of a redundancy during a multi-bank operation extends over one random access cycle to allocate the redundancy for a predetermined domain.

24. (original) The method recited in claim 18, further comprising the step of fetching address bits only when the redundancy allocation enables or disables a pass or a fail bit detection to fetch the address bits only when the bank is identified and addressed during the multi-bank operation. n.

PAGE 9/12 * RCVD AT 11/7/2005 11:56:39 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2738300 * CSID:845 892 6363 * DURATION (mm-ss):03-22